AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listing of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A symmetrically stacked inductor having at least one winding, comprising:

a plurality of conductive layers, each conductive layer including at least a pair of conductive lines defining a pair of respective portions of geometrically shaped turns of said at least one winding disposed on opposing first and second longitudinally displaced sides thereof, said portions of said turns on each said conductive layer being symmetric with respect to their position on said winding, at least a first of said plurality of conductive layers having a pair of ports formed thereon and respectively coupled to opposing ends of said at least one winding;

~~comprising at least one conductive line formed out of a symmetrical and geometric conductive layer and comprising at least one~~

an inter-metal dielectric layer disposed between each adjacent pair of said plurality of conductive layers for electrically isolating ~~each~~ said adjacent conductive layers~~, and wherein the conductive line does not intersect~~; and

a plurality of ~~vias placing between the~~ via plugs formed in each inter-metal dielectric ~~layers for~~ layer, each via plug providing electrical ~~conduction~~

connection of a conductive line on said first side of one conductive layer to a conductive line on said second side of an adjacent conductive layer.

2. (Cancelled).

3. (Cancelled).

4. (Currently amended) The symmetrically stacked inductor of claim 1, further comprising a tapped apparatus ~~between the symmetrical stacked inductors~~ connected to a conductive line on a second of said plurality of conductive layers.

5. (Currently amended) The symmetrically stacked inductor of claim 1, wherein ~~two symmetrical stacked inductors are used~~ each said conductive layer includes respective portions of a pair of geometrically shaped turns for each of two windings, each said pair of portions of geometrically shaped turns being respectively disposed symmetrically on opposing first and second longitudinally displaced sides thereof to form a single chip transformer.

6. (Currently amended) The symmetrically stacked inductor of claim 1, wherein ~~two symmetrical stacked inductors are used~~ each said conductive layer includes respective portions of a pair of geometrically shaped turns for each of three windings, each said pair of portions of geometrically shaped turns being respectively disposed symmetrically on opposing first and second longitudinally displaced sides thereof to form a single chip balun element.

7. (Cancelled).

8. (Currently amended) The symmetrically stacked inductor of claim 1, wherein said geometrically shaped turn portions on one conductive layer are of a different ~~the size of the symmetrical and geometric even conductive layer is not the same as the~~ size than said ~~of the symmetrical and~~ geometrically shaped turn portions on an adjacent ~~odd~~ conductive layer.

9. (Cancelled).

10. (Cancelled).

11. (Cancelled).

12. (New) A symmetrically stacked inductor having at least one first winding and at least one second winding, comprising:

a plurality of first conductive layers consecutively interspersed and alternating with a plurality of second conductive layers, each of said first conductive layers including at least a pair of first conductive lines defining a pair of respective portions of geometrically shaped turns of said at least one first winding disposed symmetrically on opposing first and second longitudinally displaced sides thereof, said portions of said turns on each said first conductive layer being symmetric with respect to their position on said at least one first winding, each of said second conductive layers including at least a pair of second conductive lines defining a pair of respective portions of geometrically shaped turns of said at least one second winding disposed symmetrically on opposing first and second longitudinally displaced sides thereof, said portions of said turns on each said second conductive layer being symmetric with respect to their position on said at least one second winding, at least one of each of said plurality of first and second conductive layers having a pair of ports formed thereon and respectively coupled to opposing ends of a corresponding one of said at least one first and second windings;

an inter-metal dielectric layer separating each said first conductive layer from an adjacent second conductive layer for electrical isolation thereof;

a plurality of first via plugs formed in each inter-metal dielectric layer, each first via plug providing electrical connection of a conductive line on said first side of one first conductive layer to a conductive line on said second side of another first conductive layer; and

a plurality of second via plugs formed in each inter-metal dielectric layer, each second via plug providing electrical connection of a conductive line on said first side of one second conductive layer to a conductive line on said second side of another second conductive layer.